Creating and Optimizing Interfaces for Electric-Field and Photon-Induced Charge Transfer

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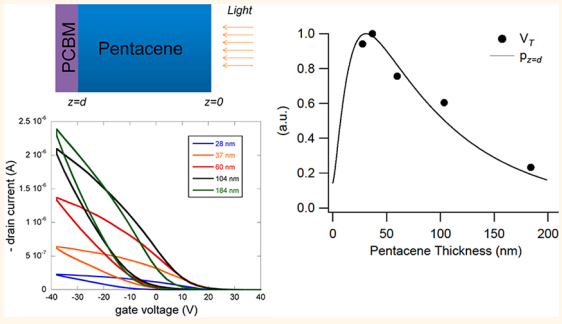
ABSTRACT We create and optimize a structurally well-defined electron donor—acceptor planar heterojunction interface in which electric-field and/or photon-induced charge transfer occurs. Electric-field-induced charge transfer in the dark and exciton dissociation at a pentacene/PCBM interface were probed by *in situ* thickness-dependent threshold voltage shift measurements in field-effect transistor devices during the formation of the interface. Electric-field-induced charge transfer at the interface in the dark is correlated with development of the pentacene accumulation layer close to PCBM, that is, including interface area, and dielectric relaxation time in PCBM. Further, we demonstrate an *in situ* test structure that allows probing of both exciton diffusion length and charge transport properties, crucial for optimizing optoelectronic devices. Competition between the optical absorption length and the exciton diffusion length in pentacene governs exciton dissociation at the interface. Charge transfer mechanisms in the dark and under illumination are detailed.



KEYWORDS: pentacene · PCBM · exciton dissociation · charge transfer · field-effect transistor

Organic semiconductors have been used to form heterojunction interfaces with alternate organic or inorganic materials for modern electronic and/or photonic device applications.[1−4] In constructing organic−organic heterojunction interfaces, charge transfer at any given interface is a central issue due to its significance for a variety of device applications such as organic solar cells (OSCs) and organic memory field-effect transistors (OMFETs).[5−8] In particular, electric-field-assisted charge trapping in an electron donor/acceptor interface has been accepted as the main source of large hysteresis in the current profile.[9,10] In OSCs, an effective power conversion efficiency is achieved through balance between photoinduced charge transfer, which leads to charge-separated states within the organic semiconductors, and charge transport.[11−13]

Bulk heterojunction interfaces have been widely adopted in memory and solar cell devices due to a wide memory window and large photocurrent arising from a larger donor/acceptor interface area in comparison with bilayer interfaces.[14−16] However, structural complexity at the bulk heterojunction interface in a memory or solar cell device inhibits understanding the mechanism of charge transfer and investigation surrounding the formation of the donor/acceptor interface. To overcome these limitations, planar heterojunction devices have been fabricated. For example, Tseng *et al.*[17] demonstrated that the charge transfer and trapping properties at a pentacene/Au nanoparticle interface can be tuned by modifying the surface properties of Au nanoparticles with a variety of self-assembled monolayers. The memory window in the field-effect transistor (FET) device was determined by the choice of self-assembled monolayer, Au particle size, and applied gate electric field. The electric-field-assisted charge transfer and trapping mechanism account for electric bistability in the device. A bilayer of pentacene/solution processed ZnO was

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structured in an FET device exhibiting nonvolatile memory elements characterized by large hysteresis.[6] Baeg *et al.*[18] fabricated organic memory FETs consisting of pentacene and polymer electret materials. They demonstrated that the electrical conductivity of one class of polymer electrets in the bottom layer dictates the charge retention time in the devices. Studies pertaining to photoinduced charge transfer in selected electron donor/acceptor combinations have also been performed.[19,20] Park *et al.*[19] described photoinduced charge transfer between pentacene and C_{60} self-assembled monolayers through evaluation of the threshold voltage shift in an FET device. The short circuit current in organic solar cells fabricated with a planar heterojunction interface was enhanced upon modification of the electron donor/acceptor interface.[21]

Despite extensive research toward the functional definition of heterojunction interfaces for OSCs and OMFETs, a systematic and comprehensive study correlating charge transfer with interface formation is lacking. Such studies could provide vital insight into the time and length scales associated with charge transfer at donor/acceptor interfaces. The choice of pentacene and PCBM as the electron donor and electron acceptor, respectively, is advantageous over alternative systems because the structural and electrical properties of these individual materials are well-known. To the best of our knowledge, electric-field and photoinduced charge transfer within this model system has not been fully investigated from the electronic and structural perspectives during interface formation in a controlled environment. Exploration of these features allows exploration of these competing components in dictating charge transfer in the dark and under illumination, input that is essential to the future design of viable materials systems for OSC and OMFET applications. Further, conventional solar cell or memory configurations in which functional layers are stacked create a series of interfaces, posing limited access into individual processes such as exciton dissociation and charge transport and extraction properties.

In this study, we created a structurally well-defined interface where electric-field-assisted and/or photoinduced charge transfer occurs. These transfer processes were probed at a pentacene/PCBM interface during interface formation through conducting channel formation *via* growth of pentacene islands on a thin PCBM layer to elucidate the charge transfer mechanism that leads to electrical bistability and/or exciton dissociation during illumination. We found that the memory window in a pentacene/PCBM memory FET is influenced by dielectric relaxation in PCBM as well as the interface area between pentacene and the C_{60} analogue, providing critical insights into the charge transfer mechanism. Significantly, we could estimate the exciton diffusion length in pentacene *via in situ* thickness-dependent electrical measurements. Thus, an electrical probe for measurement of exciton dissociation and charge transport which can be utilized in solar cell devices is provided.

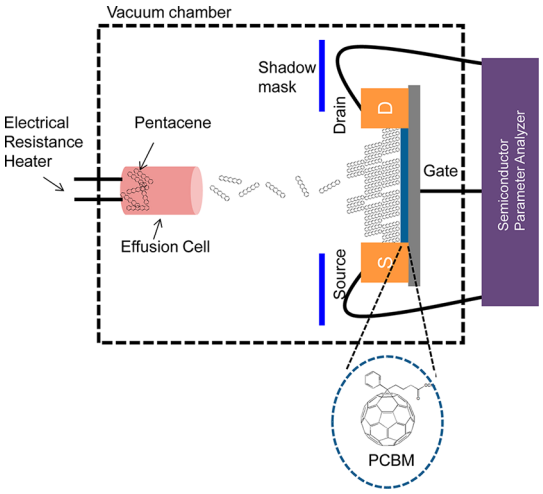

Figure 1. Schematic diagram of the experimental setup for *in situ* electrical characterization.

The selection of pentacene and PCBM, perhaps the most widely explored hole and electron transport materials, respectively, was based upon their high mobilities. Pentacene has been successfully coupled with electron-accepting fullerene derivatives which exhibit high electron affinity and tunability. Particularly, PCBM has been structured into OSCs with low band gap polymer donors, demonstrating high performance through a balance between a series of processes including charge transfer and transport. The present results provide vital perspectives for optimizing charge transfer in memory and solar cell devices and also allow for an *in situ* electrical probe for functional interfaces, in general.

RESULTS AND DISCUSSION

Pentacene/PCBM Interface Formation. Interface formation of pentacene on PCBM is achieved by vacuum deposition of pentacene molecules onto a layer of PCBM spin-coated onto a two-contact FET device, as shown in the schematic diagram in Figure 1. Structural change at the interface is characterized *via* atomic force microscopy (AFM) imaging of samples created simultaneously with samples used for electrical characterization. Figure 2a presents an AFM image of pentacene islands (bright region) on PCBM (dark region) at an initial stage of pentacene growth. Unlike pentacene deposited on SiO_2,[22] on a PCBM surface, pentacene islands grow in three dimensions, forming about 7 nm thick islands, corresponding to 4−5 molecular layers, as shown in Figure 2a.[23] With continued deposition, the pentacene islands grew both laterally and vertically, exhibiting a three-dimensional growth mode, as shown in Figure 2b. Layered pentacene islands having a molecular step size of ~1.7 nm

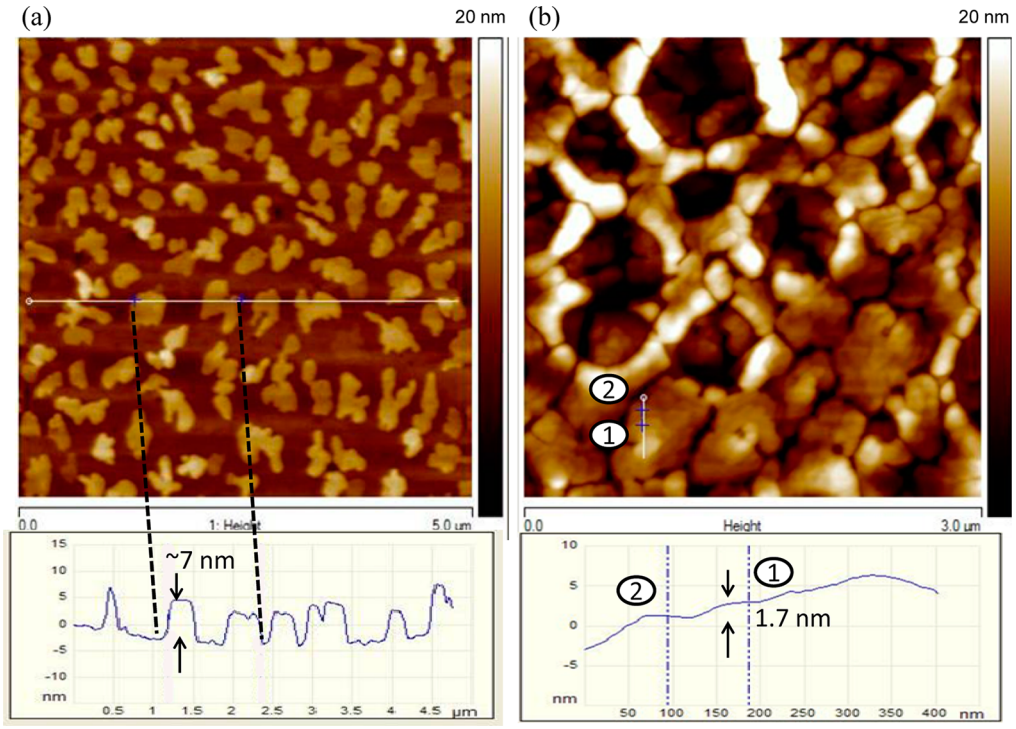

Figure 2. Tapping mode AFM height images of pentacene on PCBM as a function of time.

are poorly connected, as displayed in the inset of Figure 2b.

X-ray diffraction results for pentacene and pentacene on PCBM are shown in the Supporting Information (Figure S1). For both samples, pentacene showed two phases[24,25] corresponding to a *d* spacing of 14.6 ("bulk phase") and 15.5 Å ("thin film phase"). For the pentacene deposited on PCBM, the predominant phase was the thin film phase, while that for pentacene on SiO_2 was the bulk phase. This difference can be attributed to a difference in the interactions between pentacene and the underlying layer. XRD peaks associated with crystalline PCBM were not observed (note that the thickness of PCBM is about 5 nm.). However, when a PCBM film ~200 nm thick was constructed, diffraction peaks assigned to the crystal structure of PCBM were observed. In the case of the thin PCBM film, it is conceivable that the entire thickness of the layer is affected by interaction with the substrate leading to the formation of an amorphous film or small crystallites, whereas for the thicker sample, interactions with the substrate are minimized, allowing for the formation of a crystalline film.

Conducting Channel Formation. During pentacene growth, conducting channel formation in a pentacene FET is achieved through lateral growth of pentacene islands, creating current pathways within the pentacene film.[26] Within the framework of diffusion-mediated growth,[27,28] that accounts for the observed pentacene growth mode on PCBM (Figure 2), where incident pentacene molecules land either onto the PCBM surface or onto existing pentacene islands. Pentacene molecules on PCBM diffuse and aggregate into the existing islands, increasing their lateral size, while those on the pentacene surfaces either migrate to the PCBM lower layer or adhere to the step-edge of the pentacene islands due to an Ehrlich−Schwoebel barrier, thus affording a layered island structure.[27] Through diffusion-limited aggregation of pentacene molecules on PCBM, pentacene islands begin to coalesce, as shown in Figure 2b. Figure 3 depicts the transfer and output characteristic curves of a pentacene/PCBM FET obtained from *in situ* electrical measurements, immediately after percolation of pentacene islands. The thickness at which current onset is attained (~30 nm) is calculated from the deposition rate determined from the total thickness of pentacene islands for a given growth time. The percolation thickness is far thicker than a theoretical thickness of ~1 nm estimated from continuous two-dimensional percolation theory.[29] In the I_D-V_G measurement, the gate voltage was swept between 40 and −40 V at a drain voltage of −3 V. The gate scan rate was 1.3 V/s, far slower than the time constant of charge accumulation in a pentacene/PCBM FET estimated from the resistance of pentacene and the capacitance of the SiO_2 gate dielectric and ranging from 10^{-5} to 10^{-4} s. A large hysteresis characterized by a large threshold voltage difference of −41 V in the forward and reverse sweeps was reported previously.[30] The origin of this hysteresis was discussed in relation to charge trapping and detrapping controlled by the gate electric field at the pentacene/PCBM interface. The time constants for trapping (83 s) and detrapping (71 s) of electrons, measured from the

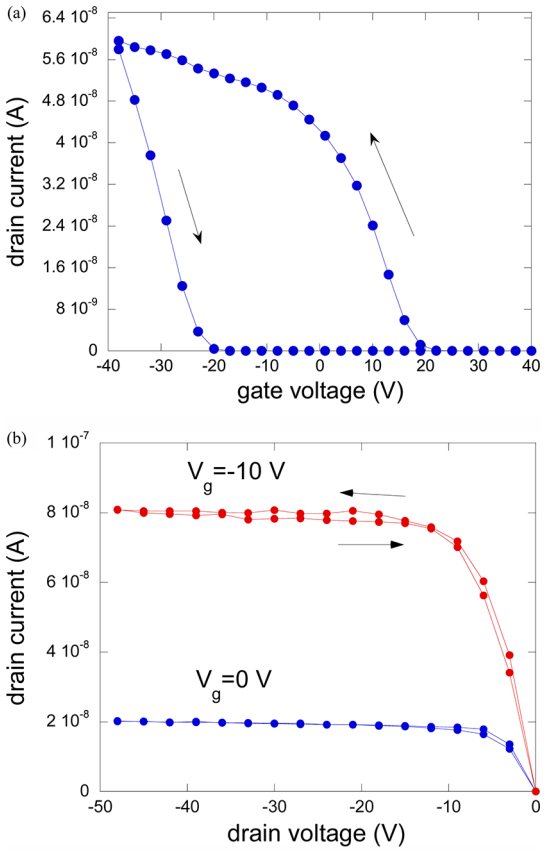

Figure 3. (a) I_D-V_G ($V_D = -3$ V) and (b) I_D-V_D curves for a pentacene/PCBM FET measured in the dark.

current transient curves, were far larger than the time constant of charge accumulation in the penatcene/PCBM FETs, the mechanism for which is discussed below. The output characteristic curves in Figure 3b, featuring the linear and saturation regions in transistor operation, ensure that the large hysteresis is associated with conduction of hole carriers in the pentacene channel.

Thickness Dependence of Electric-Field-Induced Charge Transfer at a Pentacene/PCBM Interface. The magnitude of the threshold voltage shift in the dark varies during formation of a pentacene/PCBM interface. While increasing pentacene film thickness, the threshold voltage was measured using a forward gate voltage sweep from 40 to −40 V. During the *in situ* measurements,[26,30] in which pentacene deposition is paused for electrical measurement, the number of pause/measurement cycles was limited in order to minimize perturbation in pentacene growth arising from a possible change in deposition rate. Figure 4a depicts I_D-V_G curves obtained at different stages of pentacene growth. The threshold voltage, the gate voltage required to induce mobile carriers in the conducting channel, was determined by a linear fit of the gate voltage *versus* drain current, as shown in the inset of Figure 4a. The threshold voltage measured in Figure 4a was further plotted as a function of thickness (Figure 4b), where the threshold voltage decreased with increased thickness. This result is at first puzzling because, considering the growth mode of pentacene on PCBM, it was expected that the threshold voltage would shift to a more positive value (increasing) with increasing thickness. Further, continued pentacene deposition after formation of the conducting pathways enables incoming pentacene molecules to fill the gap observed between pentacene islands grown on a PCBM/SiO_2 substrate according to the growth mode described in Figure 2. The continuous increase of the FET hole mobility in pentacene (Figure 4b1) provides evidence that the formation of a continuous conducting channel close to PCBM is not complete even at a thickness of up to ~180 nm. Recall that FET mobility is governed by the structural properties of pentacene within the charge accumulation layer having a thickness of only several molecular layers close to the gate dielectric. The FET hole mobility in pentacene was determined by I_D-V_G curves in the linear regime of transistor operation at a low drain voltage according to eq 1:

$$I_{D,linear} = \frac{W}{L}\mu C_i(V_G - V_T)V_D \qquad (1)$$

where μ represents the FET mobility of holes, C_i is the capacitance of the gate dielectric per unit area, and L and W are the channel length and width, respectively.

The continuous increase in the FET mobility observed with increased pentacene thickness up to ~180 nm cannot be ascribed to the length scale of the accumulation layer which corresponds to only several molecular layers, supporting the supposition that enhanced charge transport properties arise from improved connectivity between pentacene islands in close proximity to the PCBM interface resulting from the formation of additional percolation pathways within and between pentacene islands. Therefore, the number of electrons transferred to PCBM is expected to increase as a result of the increased interface area between the two semiconductors. The resultant increase in the space charge density, n, in the PCBM layer with increased pentacene thickness can be estimated from the relation, $n = (C_i\Delta V_T)/q$, as noted in Supporting Information Figure S6. The origin of the decrease in the threshold voltage with thickness is discussed below.

Interestingly, we observed the opposite trend for several devices (see Supporting Information Figures S4 and S5), consistent with our prediction, in which the threshold voltage increases with thickness for the reasons mentioned above. The contradiction between the two distinct results is suggested to arise from a difference in the dielectric relaxation times for the PCBM layers in the devices (Figure 4b and Figure S5), where the dielectric relaxation time is the characteristic time required to neutralize injected carriers. Charge

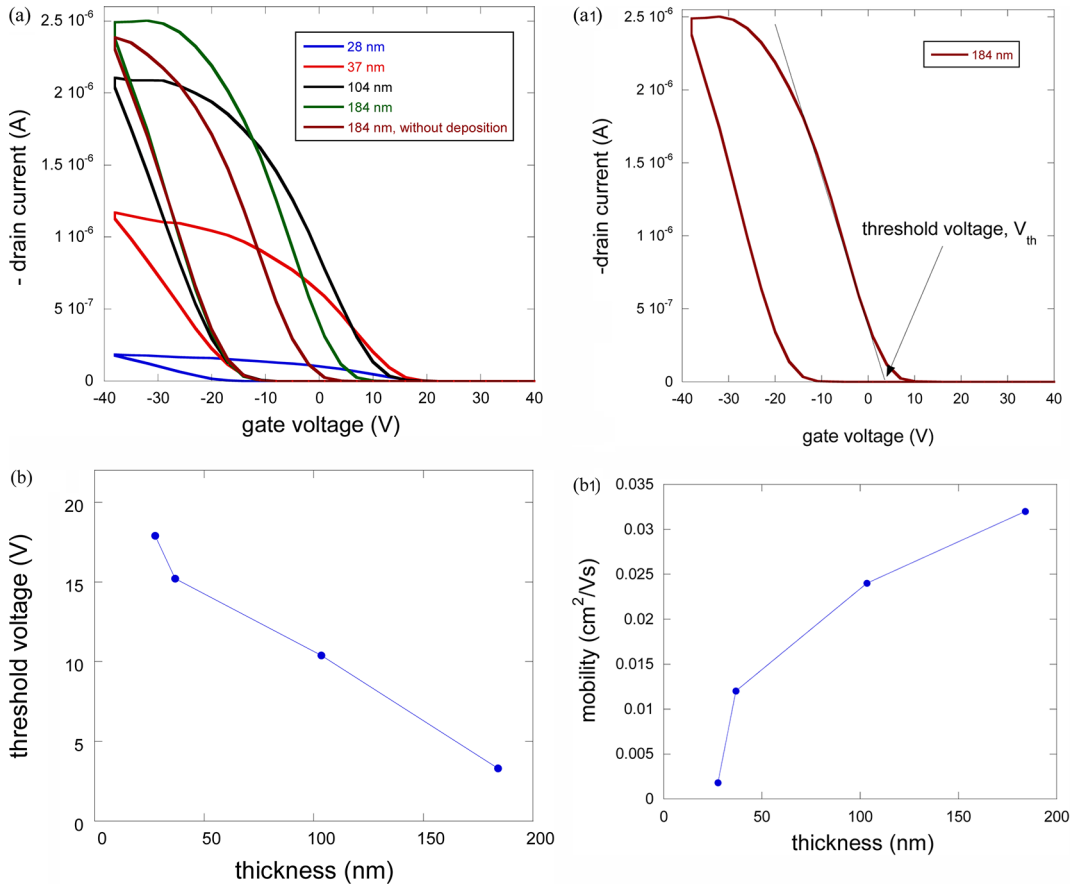

Figure 4. Gate electric-field-induced charge transfer. (a) I_D-V_G ($V_D = -3$ V) curves at different pentacene thicknesses in the dark. (a1) Threshold voltage in a forward sweep as measured from a linear fit in an I_D-V_G curve. (b) Plot of threshold voltage as a function of pentacene thickness. (b1) FET hole mobility ($V_D = -3$ V) as a function of thickness.

carriers injected into a neutral material decay exponentially as described by eq 2.

$$\sigma = \sigma_0 \exp\left(-\frac{t}{\tau_d}\right) \quad (2)$$

The dielectric relaxation time is given by $\tau_d = \rho\varepsilon_s$, where ρ is the resistivity and ε_s is the dielectric constant. As the electron resistivity of PCBM decreases, the dielectric relaxation time decreases, which is an indication that the electrons transferred into PCBM are easily neutralized, thereby shifting the threshold voltage to a more negative value. Electron current observed at $V_G = 40$ V and $V_D = -3$ V increased with time, even without further pentacene deposition (see Supporting Information S2), suggesting that the electron current originates from the n-channel semiconducting PCBM layer. Indeed, the threshold voltage continued to decrease over 3 days, even without further pentacene deposition, as shown in Figure 3a. The increased electron conductivity in the PCBM layer led to a linear decrease in the threshold voltage, as shown in Figure 4b. Thus, in the device, the decrease in dielectric relaxation time of the PCBM layer was dominant over an increase in interface area between pentacene and PCBM in determining the threshold voltage. However, for the second device (Figures S4 and S5), in which the threshold voltage increases with pentacene thickness, increase in the size of the pentacene islands that bridge the gaps between islands is dominant over the dielectric relaxation time in PCBM, resulting in an increase in the threshold voltage with thickness. It is believed that this increase results from an increase in the size of the bridging pentacene islands allowing more electrons from pentacene to be trapped in PCBM while the gate electric field is the same. Indeed, in the device, no electron current was apparent in PCBM during pentacene deposition, indicating that the transferred electrons from pentacene are trapped and immobilized in PCBM, facilitating the formation of a built-in electric field at the interface that can increase the threshold voltage. The threshold voltage remained constant after discontinuation of pentacene deposition because the threshold voltage is determined by the change in pentacene/PCBM interface area with pentacene growth, not by the dielectric relaxation time of PCBM, as seen in the Supporting Information (Figure S5). While the same parameters were used in the fabrication of the devices showing opposing trends, the charge transport properties in PCBM may vary from sample to sample because air exposure after spin-coating was unavoidable.

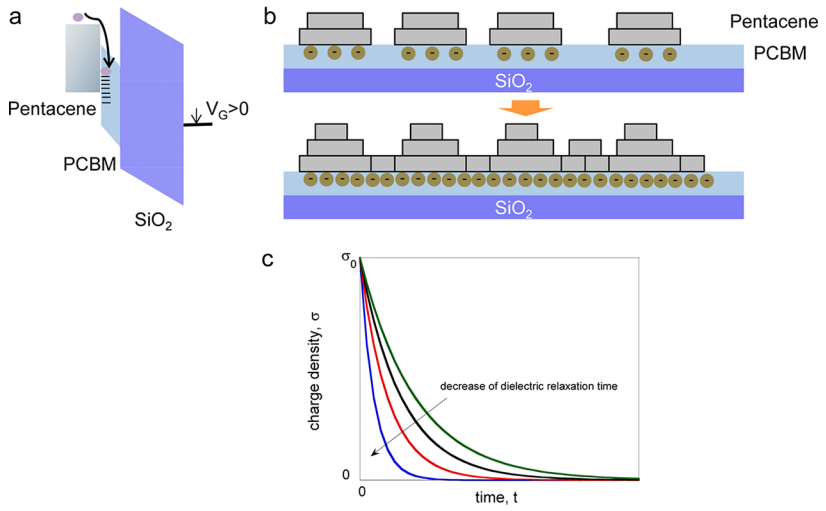

Figure 5. Schematic diagrams of (a) charge transfer mechanism at the pentacene/PCBM interface and (b) charge trapping with an increase in the pentacene/PCBM interfacial area. (c) Plot of charge density as a function of time.

These results confirm the proposed mechanism for charge transfer in which the large hysteresis observed at the interface results from charge trapping and retention of electrons transferred from pentacene.[30]

To summarize, the magnitude of the threshold voltage shift in the dark is determined by a competition between the dielectric relaxation time in PCBM and the formation of a continuous, complete, 2D accumulation layer in close proximity to the underlying PCBM layer, including factors associated with the interfacial area between the two materials. A positive gate electric field positions electrons emanating from pentacene into localized states within PCBM, shifting the threshold voltage as described in Figure 5a. As more molecules fill the gaps between the pentacene islands, more electrons per unit area can be transferred and trapped due to the increased interface area, thus enhancing carrier mobility in pentacene at the interface (Figure 5b). The schematic diagram in Figure 5b explains the increase in electron density in PCBM with the increased number of pentacene molecules. The other determinant is the dielectric relaxation time. As the electron conductivity of PCBM increases, the dielectric relaxation time decreases, accelerating charge density decay in PCBM, as depicted in Figure 5c. An increase in the charge density decay rate can reduce the number of electrons trapped in PCBM. For a systematic study of dielectric relaxation in PCBM, investigation of the temperature dependence of threshold voltage is required, elucidating the dynamics of trapped electrons and the activation energy for trapping/detrapping.

Exciton Dissociation at the Pentacene/PCBM Interface. A change in pentacene thickness can influence photoinduced charge transfer as well as electric-field-assisted charge transfer in the dark, as derived from the threshold voltage shift. An increase in pentacene thickness within its optical absorption length increases the number of photogenerated carriers. An exciton diffusion length less than the optical absorption length in pentacene limits the number of charge carriers available for photoinduced charge separation at the pentacene/PCBM interface. Figure 6a depicts FET I_D-V_G curves at a drain voltage of −3 V acquired with increasing pentacene thickness up to 184 nm during illumination at a wavelength of 620 nm. An increase in FET hole mobility with increasing thickness was observed with concomitant variations in the threshold voltage. Threshold voltage from a forward (40 to −40 V) sweep as a function of thickness is shown in Figure 6b. Unlike the trends observed in the dark, an increase in the threshold voltage with increasing pentacene thickness was observed for thicknesses between 28 and 37 nm, followed by a decrease in the threshold voltage with further increases in the thickness of the pentacene layer. This trend was reproducibly observed in both forward and reverse sweeps. We hypothesize that the increase in the threshold voltage for pentacene thicknesses ranging from 28 to 37 nm is due to the increase in photogenerated electron−hole pairs (excitons) caused by increased light absorption, which is directly related to the thickness. The increased number of excitons within the exciton diffusion length of the pentacene film allows for an increase in the number of available carriers that can be separated at the interface. The initial increase in the threshold voltage up to a thickness of 37 nm is countered by a decrease of the threshold voltage due to thickness growth beyond the exciton diffusion length. The photoinduced threshold voltage up to about 40 nm is a compromise between optical absorption and exciton diffusion lengths, producing a peak threshold voltage at 37 nm. To quantify the relation between the two characteristic lengths, we used a model in which photoresponse in a pentacene film is simulated as a function of thickness.[31] In the schematic diagram shown in Figure 7a, incident photons create excitons

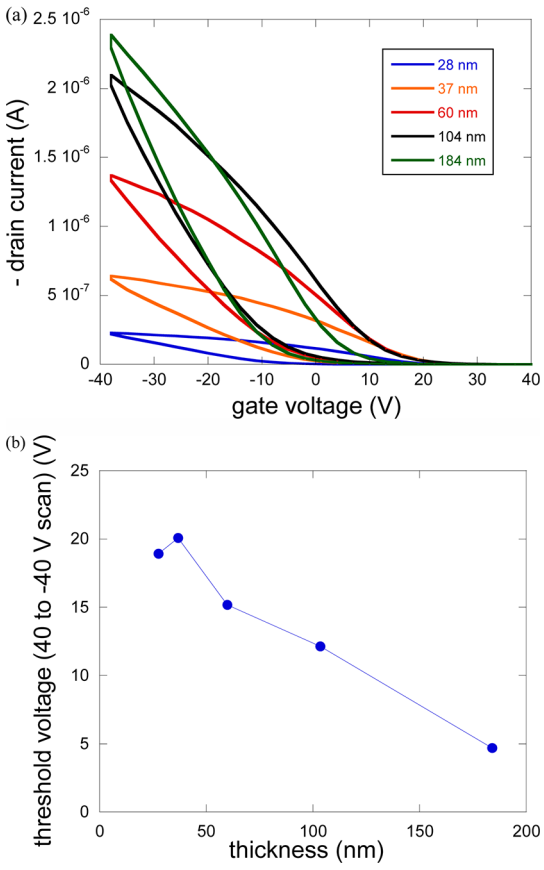

Figure 6. Photoiduced threshold voltage shift in a pentacene/PCBM FET. (a) I_D–V_G (V_D = −3 V) curves at different pentacene thicknesses under illumination at a wavelength of 620 nm. (b) Plot of threshold voltage as a function of thickness.

in both the pentacene adjacent to PCBM and in the bulk of the pentacene layer. Exciton density from the surface ($z = 0$) to the interface between pentacene and PCBM ($z = d$), $n(z,t)$, can be given by

$$\frac{\partial n(z,t)}{\partial t} = D_{ecs}\frac{\partial^2 n(z,t)}{\partial z^2} - \tau_{exc}^{-1} n(z,t) + g I_0 e^{-\alpha z}$$

where D_{exc} is the exciton diffusion coefficient, τ_{exc} the exciton lifetime, g the light absorption efficiency, I_0 the incident light intensity, α the absorption coefficient, z the distance from the surface. The exciton lifetime is finite because excitons are either separated at the interface or recombined in the bulk, determining the exciton diffusion length, $L_{exc} = (D_{exc}\tau_{exc})^{1/2}$. Holes injected into pentacene due to exciton dissociation at the interface contribute to the photocurrent, along with excitons in the bulk. The injected hole density $h(z,t)$ is given by

$$\frac{\partial \hat{h}(z,t)}{\partial t} = D_{\hat{h}}\frac{\partial^2 \hat{h}(z,t)}{\partial z^2} - \tau_{\hat{h}}^{-1}\hat{h}(z,t)$$

where D_h is the diffusion coefficient of the hole and τ_h is the lifetime of the hole. In the model, exciton flux at a pentacene/PCBM junction is assumed to be equal to

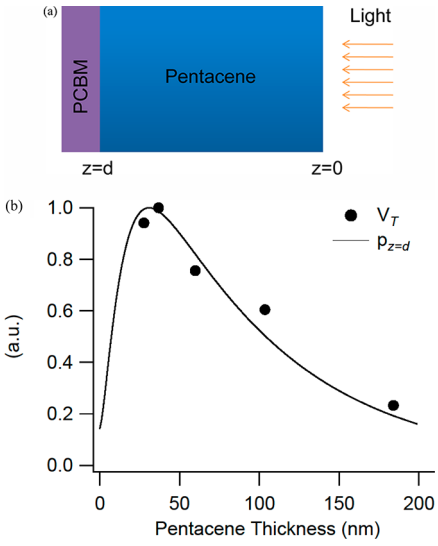

Figure 7. (a) Schematic diagram of the photocurrent generation model. (b) Plot of normalized excess hole concentration (p_z) as a function of pentacene thickness. Normalized FET threshold voltages fits to p_z, the concentration of hole carriers injected into pentacene due to exciton dissociation at the interface. The best fit was found for an exciton diffusion length of 25 nm and optical absorption length of approximately 83 nm.

exciton dissociation velocity, v_{dis}, indicating that all excitons at the interface are dissociated, as given in the relation

$$D_{exc}\frac{\partial n(d)}{\partial z} = v_{dis} n(d)$$

The exciton and hole concentration gradients are assumed to be zero at the interface. Further, excitons are dissociated at the pentacene/PCBM interface ($z = d$), as described by

$$D_h\frac{\partial h(d)}{\partial z} = -D_{exc}\frac{\partial n(d)}{\partial z}$$

Using the boundary conditions described above, the photogenerated excess hole density at the pentacene–PCBM interface as a function of pentacene thickness z was calculated. The model parameters were fit to the experimental values, producing an exciton diffusion length of 25 nm. This value is within the range of 7 and 65 nm reported in previous studies.[32,33] In the model, the internal electric field in pentacene is assumed to be negligible, validated by the bias conditions used in the experiments in which the magnitude of the gate electric field (~2×10^6 V/cm) voltage is far larger than the lateral electric field (3×10^3 V/cm) between the source and drain electrodes. Further, pentacene is a typical p-channel semiconductor. While electron conduction has been found in some previous studies, electron mobility is reported to be very low compared with hole mobility. Additionally, the electrical contact resistance between pentacene and Au was found not to be significant compared with charge transport in the pentacene channel, as shown in

Supporting Information Figure S7. The potential profile along the pentacene channel is almost linear, and the voltage drops at the source and drain electrodes were estimated based on a linear fit of the potentials measured using a FET device with multiple voltage probes along the channel.[34,35] The voltage drops were less than 0.5 V, far smaller than the applied drain voltage (5 V), indicating that the threshold voltage measured here is not determined by the electrical contact properties but rather by charge transfer between pentacene and PCBM.

However, it is noted that the electrons trapped in the localized states between the lowest unoccupied molecular orbital and the highest occupied molecular orbital of PCBM can be detrapped during illumination with a wavelength of 620 nm, affecting the magnitude of the threshold voltage because an increase in the electrical conductivity in the PCBM layer can shorten the dielectric relaxation time. In our experiments, the effect of detrapped electrons on the threshold voltage change is thought to be more significant in a thinner pentacene film because optical absorption in the PCBM layer decreases with increasing pentacene thickness. Once the pentacene thickness increases from 28 to 37 nm, more electrons will be trapped in the underlying PCBM by photoexcitation in the thicker pentacene film. However, in the case where detrapping in the PCBM layer is dominant, the threshold voltage will not increase in the region, forming a peak, because the dielectric relaxation time at 37 nm is shorter than that at 28 nm due to enhanced electron conductivity, as shown in Supporting Information Figure S2. In other words, the electrical resistance of the PCBM layer is the highest near the pentacene thickness at which percolation occurs, suggesting that the electron mobility is extremely low, mitigating the effect, if any, of detrapping of electrons on the threshold voltage. This perspective is supported by the experiment using a C_{60}-terminated self-assembled monolayer (SAM) as an electron-accepting layer (see Supporting Information Figure S8), the conductivity of which is far lower than the PCBM layer, preventing electron transport of detrapped electrons in the C_{60}-terminated SAM. The threshold voltage shift as a function of pentacene thickness was fitted to the model, producing an exciton diffusion length of 10 nm, comparable with that of PCBM. These considerations allow us to claim that the threshold voltage change arising from hopping of detrapped electrons, if any, within PCBM is not significant.

To summarize, a characteristic peak observed at a thickness of about 28 nm explains that the exciton diffusion length in pentacene is shorter than the optical absorption length. Below 28 nm, most of the excitons are separated, forming charge transfer states near the interface, while excitons generated at the surface of a thicker pentacene film recombine before reaching the interface. The competition between exciton diffusion and optical absorption is applied to a C_{60}-terminated SAM as an electron-accepting layer, as discussed earlier.

SUMMARY AND CONCLUSIONS

We created and probed a structurally well-defined interface where electric-field and/or photon-induced charge transfer occurs. Increase in interfacial area, accompanied by concomitant increase in the carrier mobility as a result of formation of more conducting pathways, increases the number of charge carriers transferred in the dark. Dielectric relaxation time in materials is crucial in controlling charge retention. In the presence of light, to maximize the photocurrent resulting from photoinduced charge separation at the interface, a good balance between optical absorption and diffusion length is crucial. Our approach, in which photoinduced charge separation can be probed using *in situ* threshold voltage measurements, can be adapted to optimize exciton dissociation in buried interfaces of a composite film in solar cell devices. The short circuit current in bulk heterojunction solar cell devices can be enhanced by controlling, at the nanoscale, the optimum thickness where the number of excitons dissociated at the interface is maximized. Our method that adopts the FET geometry coupled with *in situ* measurement to probe time and length scales associated with charge transfer can be universally applied to optimize both charge transport and photoinduced charge transfer at functional interfaces embedded in optoelectronic or memory devices.

EXPERIMENTAL SECTION

A pentacene/PCBM FET was fabricated on a 200 nm thick SiO_2 substrate as a gate dielectric. Source and drain metal [Au (60 nm)/Cr (~5 nm)] electrodes were spaced by a channel length of 10 μm and width of 2 mm. The detailed description of the FET device fabrication process and associated materials processing has been described previously.[31] The FET device coated with a layer of PCBM was transferred into a vacuum chamber immediately after preparation of the semiconducting layer for *in situ* electrical measurements during pentacene deposition. The output and transfer characteristic curves of the pentacene/PCBM FET in the dark and under illumination were measured as a function of pentacene thickness using a semiconductor parameter analyzer (HP4155C). A red laser light source having a wavelength of 620 nm was incident through a quartz window built into the vacuum chamber to excite the pentacene upper layer, selectively suppressing optical absorption in PCBM. Through comparison of the morphology of the pentacene films at different thicknesses, we examined the growth mode of pentacene on PCBM. Height images from tapping mode atomic force microscopy were used to study pentacene growth.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Pentacene/PCBM FET characterization (Figures S1–S8). This material is available free of charge *via* the Internet at http://pubs.acs.org.

REFERENCES AND NOTES

1. Ren, S. Q.; Zhao, N.; Crawford, S. C.; Tambe, M.; Bulovic, V.; Gradecak, S. Heterojunction Photovoltaics Using GaAs Nanowires and Conjugated Polymers. *Nano Lett.* **2011**, *11*, 408–413.
2. Colvin, V. L.; Schlamp, M. C.; Alivisatos, A. P. Light-Emitting-Diodes Made from Cadmium Selenide Nanocrystals and a Semiconducting Polymer. *Nature* **1994**, *370*, 354–357.
3. Goh, C.; Scully, S. R.; McGehee, M. D. Effects of Molecular Interface Modification in Hybrid Organic–Inorganic Photovoltaic cells. *J. Appl. Phys.* **2007**, *101*, 114503.
4. Hang, H. T.; Guo, X. F.; Hui, J. S.; Hu, S. X.; Xu, W.; Zhu, D. B. Interface Engineering of Semiconductor/Dielectric Heterojunctions toward Functional Organic Thin-Film Transistors. *Nano Lett.* **2011**, *11*, 4939–4946.
5. Mabrook, M. F.; Yun, Y. J.; Pearson, C.; Zeze, D. A.; Petty, M. C. A Pentacene-Based Organic Thin Film Memory Transistor. *Appl. Phys. Lett.* **2009**, *94*, 173302.
6. Pal, B. N.; Trottman, P.; Sun, J.; Katz, H. E. Solution-Deposited Zinc Oxide and Zinc Oxide/Pentacene Bilayer Transistors: High Mobility n-Channel, Ambipolar and Nonvolatile Devices. *Adv. Funct. Mater.* **2008**, *18*, 1832–1839.
7. Bredas, J. L.; Norton, J. E.; Cornil, J.; Coropceanu, V. Molecular Understanding of Organic Solar Cells: The Challenges. *Acc. Chem. Res.* **2009**, *42*, 1691–1699.
8. Zhu, X. Y.; Yang, Q.; Muntwiler, M. Charge-Transfer Excitons at Organic Semiconductor Surfaces and Interfaces. *Acc. Chem. Res.* **2009**, *42*, 1779–1787.
9. Yang, Y.; Ouyang, J.; Ma, L. P.; Tseng, R. J. H.; Chu, C. W. Electrical Switching and Bistability in Organic/Polymeric Thin Films and Memory Devices. *Adv. Funct. Mater.* **2006**, *16*, 1001–1014.
10. Ouyang, J. Y.; Chu, C. W.; Sieves, D.; Yang, Y. Electric-Field-Induced Charge Transfer between Gold Nanoparticle and Capping 2-Naphthalenethiol and Organic Memory Cells. *Appl. Phys. Lett.* **2005**, *86*, 123507.
11. Nelson, J. Organic Photovoltaic Films. *Curr. Opin. Solid State Mater. Sci.* **2002**, *6*, 87–95.
12. Facchetti, A. π-Conjugated Polymers for Organic Electronics and Photovoltaic Cell Applications. *Chem. Mater.* **2011**, *23*, 733–758.
13. Hoppe, H.; Sariciftci, N. S. Organic Solar Cells: An Overview. *J. Mater. Res.* **2004**, *19*, 1924–1945.
14. Gao, Y. R.; Ma, T. L. Bulk Heterojunction Polymer Solar Cells. *Prog. Chem.* **2011**, *23*, 991–1013.
15. Saunders, B. R.; Turner, M. L. Nanoparticle-Polymer Photovoltaic Cells. *Adv. Colloid Interface Sci.* **2008**, *138*, 1–23.
16. Blom, P. W. M.; Mihailetchi, V. D.; Koster, L. J. A.; Markov, D. E. Device Physics of Polymer: Fullerene Bulk Heterojunction Solar Cells. *Adv. Mater.* **2007**, *19*, 1551–1566.
17. Tseng, C. W.; Tao, Y. T. Electric Bistability in Pentacene Film-Based Transistor Embedding Gold Nanoparticles. *J. Am. Chem. Soc.* **2009**, *131*, 12441–12450.
18. Baeg, K. J.; Noh, Y. Y.; Ghim, J.; Lim, B.; Kim, D. Y. Polarity Effects of Polymer Gate Electrets on Non-volatile Organic Field-Effect Transistor Memory. *Adv. Funct. Mater.* **2008**, *18*, 3678–3685.
19. Park, B.; Paoprasert, P.; In, I.; Zwickey, J.; Colavita, P. E.; Hamers, R. J.; Gopalan, P.; Evans, P. G. Functional Self-Assembled Monolayers for Optimized Photoinduced Charge Transfer in Organic Field Effect Transistors. *Adv. Mater.* **2007**, *19*, 4353–4357.
20. Deibel, C.; Strobel, T.; Dyakonov, V. Role of the Charge Transfer State in Organic Donor–Acceptor Solar Cells. *Adv. Mater.* **2010**, *22*, 4097–4111.
21. Monson, T. C.; Lloyd, M. T.; Olson, D. C.; Lee, Y. J.; Hsu, J. W. P. Photocurrent Enhancement in Polythiophene- and Alkanethiol-Modified ZnO Solar Cells. *Adv. Mater.* **2008**, *20*, 4755–4759.
22. Mayer, A. C.; Ruiz, R.; Headrick, R. L.; Kazimirov, A.; Malliaras, G. G. Early Stages of Pentacene Film Growth on Silicon Oxide. *Org. Electron.* **2004**, *5*, 257–263.
23. Heringdorf, F. J. M. Z.; Reuter, M. C.; Tromp, R. M. Growth Dynamics of Pentacene Thin Films. *Nature* **2001**, *412*, 517–520.
24. Cha, S. H.; Park, A.; Lee, K. H.; Im, S.; Lee, B. H.; Sung, M. M. Pentacene Thin-Film on Organic/Inorganic Nanohybrid Dielectrics for ZnO Charge Injection Memory Transistor. *Org. Electron.* **2010**, *11*, 159–163.
25. Gundlach, D. J.; Lin, Y. Y.; Jackson, T. N.; Nelson, S. F.; Schlom, D. G. Pentacene Organic Thin-Film Transistors—Molecular Ordering and Mobility. *IEEE Electron Device Lett.* **1997**, *18*, 87–89.
26. Park, B. N.; Seo, S.; Evans, P. G. Channel Formation in Single-Monolayer Pentacene Thin Film Transistors. *J. Phys. D Appl. Phys.* **2007**, *40*, 3506–3511.
27. Ruiz, R.; Nickel, B.; Koch, N.; Feldman, L. C.; Haglund, R. F., Jr.; Kahn, A.; Family, F.; Scoles, G. Dynamic Scaling, Island Size Distribution, and Morphology in the Aggregation Regime of Submonolayer Pentacene Films. *Phys. Rev. Lett.* **2003**, *91*, 136102.
28. Tejima, M.; Kita, K.; Kyuno, K.; Toriumi, A. Study on the Growth Mechanism of Pentacene Thin Films by the Analysis of Island Density and Island Size Distribution. *Appl. Phys. Lett.* **2004**, *85*, 3746–3748.
29. Sreenivasan, S.; Baker, D. R.; Paul, G.; Stanley, H. E. The Approximate Invariance of the Average Number of Connections for the Continuum Percolation of Squares at Criticality. *Physica A* **2003**, *320*, 34–40.
30. Park, B.; Choi, S.; Graham, S.; Reichmanis, E. Memory and Photovoltaic Elements in Organic Field Effect Transistors with Donor/Acceptor Planar-Hetero Junction Interfaces. *J. Phys. Chem. C* **2012**, *116*, 9390–9397.
31. Kerp, H. R.; Donker, H.; Koehorst, R. B. M.; Schaafsma, T. J.; van Faassen, E. E. Exciton Transport in Organic Dye Layers for Photovoltaic Applications. *Chem. Phys. Lett.* **1998**, *298*, 302–308.
32. Huang, J. S.; Yang, Y. Origin of Photomultiplication in C-60 Based Devices. *Appl. Phys. Lett.* **2007**, *91*, 203505.
33. Yoo, S.; Domercq, B.; Kippelen, B. Efficient Thin-Film Organic Solar Cells Based on Pentacene/C-60 Heterojunctions. *Appl. Phys. Lett.* **2004**, *85*, 5427–5429.
34. Pesavento, P. V.; Chesterfield, R. J.; Newman, C. R.; Frisbie, C. D. Gated Four-Probe Measurements on Pentacene Thin-Film Transistors: Contact Resistance as a Function of Gate Voltage and Temperature. *J. Appl. Phys.* **2004**, *96*, 7312–7324.
35. Park, B.; Aiyar, A.; Hong, J. I.; Reichmanis, E. Electrical Contact Properties between the Accumulation Layer and Metal Electrodes in Ultrathin Poly(3-hexylthiophene)-(P3HT) Field Effect Transistors. *ACS Appl. Mater. Interfaces* **2011**, *3*, 1574–1580.